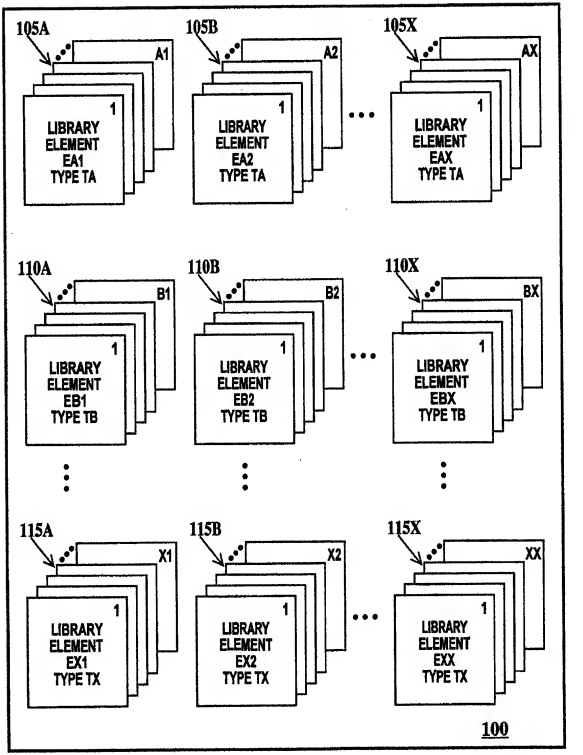
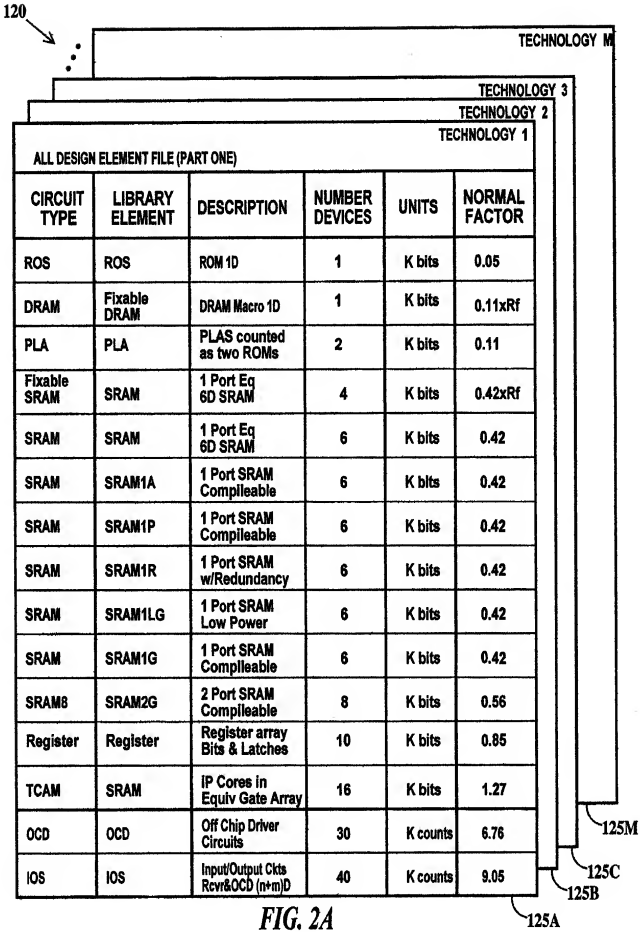

105A
A1
1
LIBRARY ELEMENT EA1 TYPE TA
105B
A2
1
LIBRARY ELEMENT EA2 TYPE TA
105X
AX
1
LIBRARY ELEMENT EAX TYPE TA
110A
B1
1
LIBRARY ELEMENT EB1 TYPE TB
110B
B2
1
LIBRARY ELEMENT EB2 TYPE TB
110X
BX
1
LIBRARY ELEMENT EBX TYPE TB
115A
X1
1
LIBRARY ELEMENT EX1 TYPE TX
115B
X2
1
LIBRARY ELEMENT EX2 TYPE TX
115X
XX
1
LIBRARY ELEMENT EXX TYPE TX
100

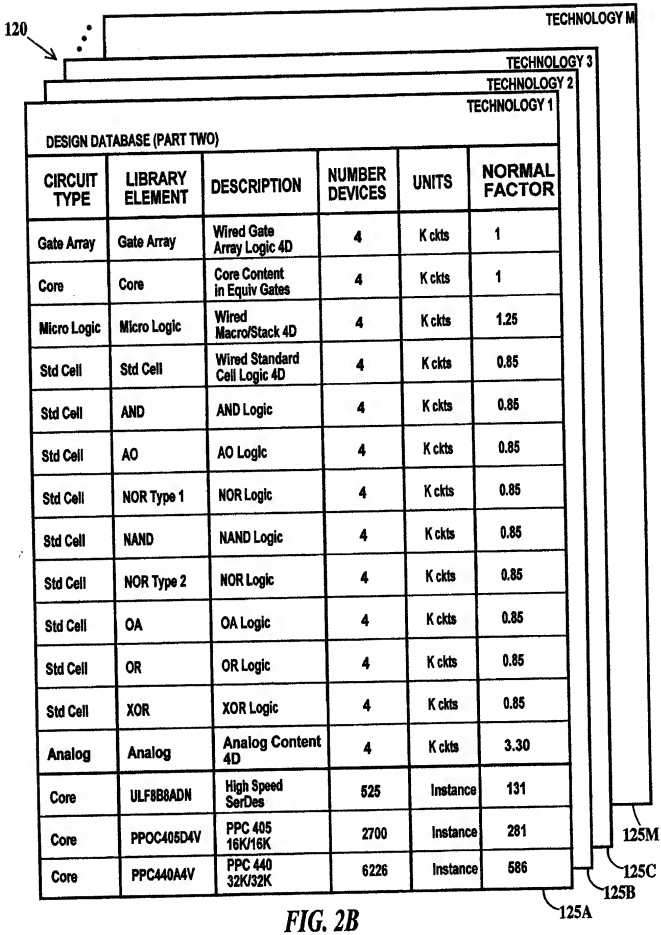
FIG. 1



ALL DESIGN ELEMENT FILE (PART ONE)

CIRCUIT TYPE	LIBRARY ELEMENT	DESCRIPTION	NUMBER DEVICES	UNITS	NORMAL FACTOR
ROS	ROS	ROM 1D	1	K bits	0.05
DRAM	Fixable DRAM	DRAM Macro 1D	1	K bits	0.11xRf
PLA	PLA	PLAS counted as two ROMs	2	K bits	0.11
Fixable SRAM	SRAM	1 Port Eq 6D SRAM	4	K bits	0.42xRf
SRAM	SRAM	1 Port Eq 6D SRAM	6	K bits	0.42
SRAM	SRAM1A	1 Port SRAM Compileable	6	K bits	0.42
SRAM	SRAM1P	1 Port SRAM Compileable	6	K bits	0.42
SRAM	SRAM1R	1 Port SRAM w/Redundancy	6	K bits	0.42
SRAM	SRAM1LG	1 Port SRAM Low Power	6	K bits	0.42
SRAM	SRAM1G	1 Port SRAM Compileable	6	K bits	0.42
SRAM8	SRAM2G	2 Port SRAM Compileable	8	K bits	0.56
Register	Register	Register array Bits & Latches	10	K bits	0.85
TCAM	SRAM	IP Cores in Equiv Gate Array	16	K bits	1.27
OCD	OCD	Off Chip Driver Circuits	30	K counts	6.76
IOS	IOS	Input/Output Ckts Rcvr&OCD (n+m)D	40	K counts	9.05

FIG. 2A



DESIGN DATABASE (PART TWO)

CIRCUIT TYPE	LIBRARY ELEMENT	DESCRIPTION	NUMBER DEVICES	UNITS	NORMAL FACTOR
Gate Array	Gate Array	Wired Gate Array Logic 4D	4	K ckts	1
Core	Core	Core Content in Equiv Gates	4	K ckts	1
Micro Logic	Micro Logic	Wired Macro/Stack 4D	4	K ckts	1.25
Std Cell	Std Cell	Wired Standard Cell Logic 4D	4	K ckts	0.85
Std Cell	AND	AND Logic	4	K ckts	0.85
Std Cell	AO	AO Logic	4	K ckts	0.85
Std Cell	NOR Type 1	NOR Logic	4	K ckts	0.85
Std Cell	NAND	NAND Logic	4	K ckts	0.85
Std Cell	NOR Type 2	NOR Logic	4	K ckts	0.85
Std Cell	OA	OA Logic	4	K ckts	0.85
Std Cell	OR	OR Logic	4	K ckts	0.85
Std Cell	XOR	XOR Logic	4	K ckts	0.85
Analog	Analog	Analog Content 4D	4	K ckts	3.30
Core	ULF8B8ADN	High Speed SerDes	525	Instance	131
Core	PPOC405D4V	PPC 405 16K/16K	2700	Instance	281
Core	PPC440A4V	PPC 440 32K/32K	6226	Instance	586

FIG. 2B

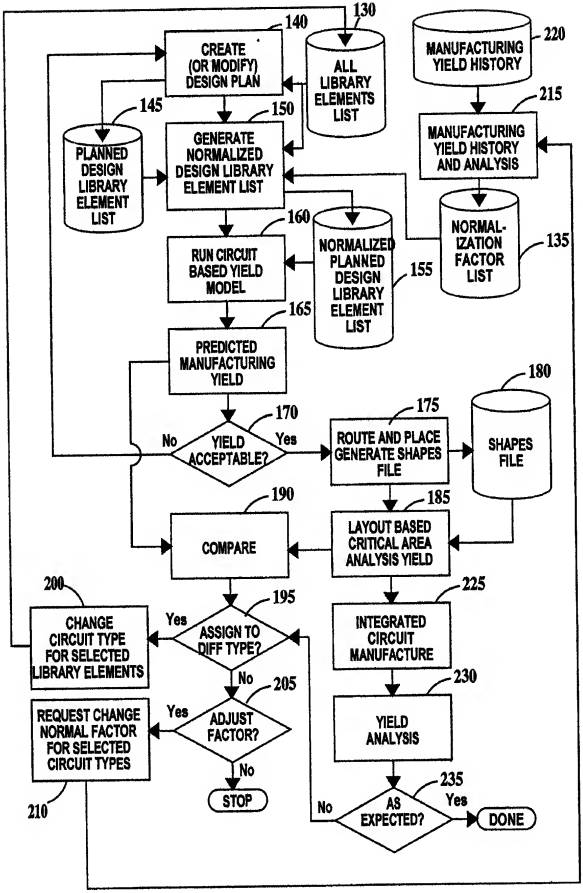

130
140
CREATE (OR MODIFY) DESIGN PLAN
ALL LIBRARY ELEMENTS LIST
MANUFACTURING YIELD HISTORY
220
145
150
215
PLANNED DESIGN LIBRARY ELEMENT LIST
GENERATE NORMALIZED DESIGN LIBRARY ELEMENT LIST
MANUFACTURING YIELD HISTORY AND ANALYSIS
160
155
135
RUN CIRCUIT BASED YIELD MODEL
NORMALIZED PLANNED DESIGN LIBRARY ELEMENT LIST
NORMAL-IZATION FACTOR LIST
165
PREDICTED MANUFACTURING YIELD
180
170
175
No
YIELD ACCEPTABLE?
Yes
ROUTE AND PLACE GENERATE SHAPES FILE
SHAPES FILE
190
185
COMPARE
LAYOUT BASED CRITICAL AREA ANALYSIS YIELD
200
195
225
CHANGE CIRCUIT TYPE FOR SELECTED LIBRARY ELEMENTS
Yes
ASSIGN TO DIFF TYPE?
INTEGRATED CIRCUIT MANUFACTURE
No
205
230
REQUEST CHANGE NORMAL FACTOR FOR SELECTED CIRCUIT TYPES
Yes
ADJUST FACTOR?
YIELD ANALYSIS
No
235
STOP
No
AS EXPECTED?
Yes
DONE
210

FIG. 3

155

NORMALIZED PLANNED DESIGN LIBRARY ELEMENT LIST				
LIBRARY ELEMENT	CIRCUIT COUNT	CIRCUIT TYPE	NORMALIZATION FACTOR	EQUIVALENT CIRCUIT COUNT
EA1	1000	TA	.5	500
EA2	1000	TA	.5	500
EB1	500	TB	.75	375
EB3	200	TB	.75	150
EB10	100	TB	.75	75
EC2	10	TC	2.5	25
EC3	20	TC	2.5	50
ED1	200	TD	.5	100
ED4	150	TD	.5	75
TOTAL	4950			1850

FIG. 4

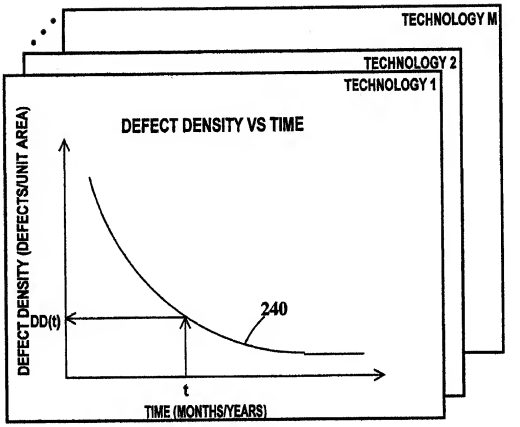

TECHNOLOGY M
TECHNOLOGY 2
TECHNOLOGY 1
DEFECT DENSITY VS TIME
DEFECT DENSITY (DEFECTS/UNIT AREA)
DD(t)
240
t
TIME (MONTHS/YEARS)

FIG. 5

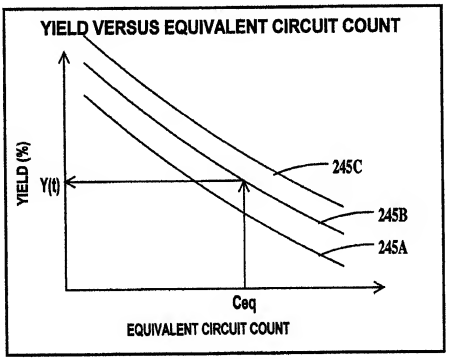

YIELD VERSUS EQUIVALENT CIRCUIT COUNT
YIELD (%)
Y(t)
245C
245B
245A
Ceq
EQUIVALENT CIRCUIT COUNT

FIG. 6

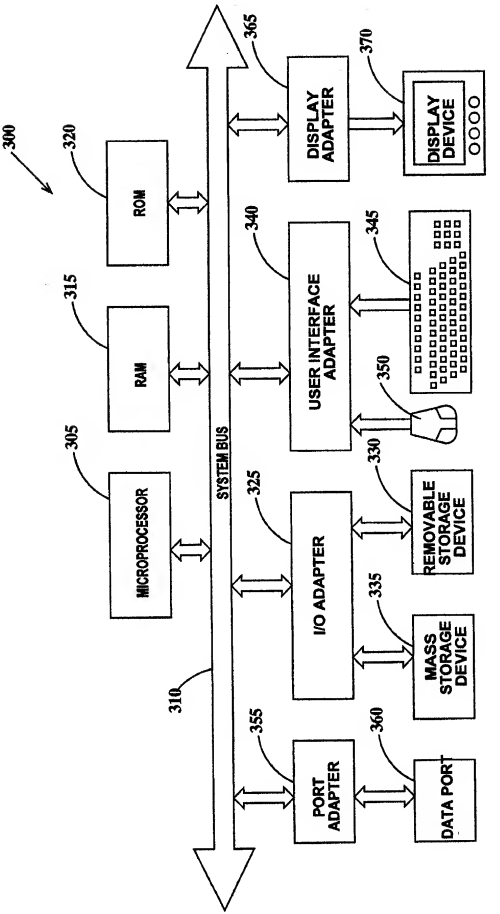

300
320
ROM
315
RAM
305
MICROPROCESSOR
310
SYSTEM BUS
365
DISPLAY ADAPTER
370
DISPLAY DEVICE
340
USER INTERFACE ADAPTER
345
350
325
I/O ADAPTER
330
REMOVABLE STORAGE DEVICE
335
MASS STORAGE DEVICE
355
PORT ADAPTER
360
DATA PORT

FIG. 7